Abstract of the Disclosure

A method for fabricating a power semiconductor device having a trench gate structure is provided. An epitaxial layer of a first conductivity type having a low concentration and a body region of a second conductivity type are sequentially formed on a semiconductor substrate of the first conductivity type having a high concentration. An oxide layer pattern is formed on the body region. A first trench is formed using the oxide layer pattern as an etching mask to perforate a predetermined portion of the body region having a first thickness. A body contact region of the second conductivity type having a high concentration is formed to surround the first trench by impurity ion implantation using the oxide layer pattern as an ion implantation mask. First spacer layers are formed to cover the sidewalls of the first trench and the sidewalls of the oxide layer pattern. A second trench is formed using the oxide layer pattern and the first spacer layers as etching masks to perforate a predetermined portion of the body region having a second thickness greater than the first thickness. A source region of the first conductivity type having a high concentration is formed to surround the second trench by impurity ion implantation using the oxide layer pattern and the first spacer layers as ion implantation masks. Second spacer layers are formed to cover the sidewalls of the second trench and the sidewalls of the first spacer layers. A third trench is formed to a predetermined depth of the epitaxial layer using the oxide layer pattern, the first spacer layers, and the second spacer layers as etching masks. A gate insulating layer is formed in the third trench. A gate conductive pattern is formed in the gate insulating layer. An oxide layer is formed on the gate conductive layer pattern. The first and second spacer layers are removed. A first metal electrode layer is formed to be electrically connected to the source region and the body contact region. A second metal electrode layer is formed to be electrically connected to the gate conductive layer pattern. A third metal electrode layer is formed to be electrically connected to the semiconductor substrate.